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2/9/07  
September 27, 2007

Commissioner for Patents  
PO Box 1450  
Alexandria, VA 22313-1450


Re: **CERTIFICATE OF CORRECTION**  
U. S. Letters Patent No. 7,089,367  
Issued: August 8, 2006  
For: **REDUCING MEMORY ACCESS LATENCIES  
FROM A BUS USING PRE-FETCHING AND  
CACHING**  
Inventor: Koker, et al.  
Our File No. 42390.P6725

Dear Sir:

Enclosed is the Certificate of Correction (two copies) for the above-referenced patent.  
This request for correction is made under rule 322 of the Rules of Practice and 35 U.S.C.  
Section 254.  
Enclosed is a copy of the allowed claim from the entered amendment filed on March 14,  
2005.

Respectfully submitted,

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP

  
Edwin H. Taylor  
Reg. No. 25,129

EHT/sn  
Enclosures

**UNITED STATES PATENT AND TRADEMARK OFFICE**  
**CERTIFICATE OF CORRECTION**

**PATENT NO.** : 7,089,367  
**DATED** : August 8, 2006  
**INVENTOR(S)** : Koker et al.

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

In column 6, at line 40, delete "CYCLE" and insert --CYCLE1--.

In column 9, at line, 28, delete "9" and insert --8--.

Delete claim 8, and insert the following claim -- An apparatus comprising: a pre-fetcher to pre-fetch a plurality of data from a memory to a data queue in response to a request; a queue controller coupled to the data queue and the pre-fetcher to deliver the pre-fetched data from the data queue to a bus independently of the memory; a data coherence controller coupled to the pre-fetcher to provide a purge signal when the request corresponds to a cache miss; and a scheduler coupled to the data coherence controller to store entries corresponding to the request, the entries being marked according to the purge signal from the data coherence controller, the marked entries corresponding to data to be purged.--.

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**PATENT NO.** 7,089,367

**Certificate of Correction (PTO Form 1050)-Amended**